

(3 Hours)

[Total Marks: 80

- N.B.: (1) Question No. 1 is **compulsory**.  
 (2) Solve any **three** questions out of remaining **five**.  
 (3) Figures to **right** indicate **full** marks.  
 (4) Assume suitable **data** where **necessary**.

- Q1** Solve any **four** (20)
- What are the important features of differential amplifier, also states its types.
  - State De'sMorgon theorem & implement OR gate using NAND gate only.
  - ADD  $(83)_{10}$  &  $(34)_{10}$  in **BCD**.
  - Convert S-R flip flop to D flip-flop.
  - State advantages & disadvantages of multiplexer.
  - Explain VHDL format in brief.
- Q2.** A) Simplify the following using Quine-Mcclusky method (10)  

$$F(A,B,C,D) = \sum m(0,3,4,11,15) + d(1,2,5)$$
- B) Design & implement one digit BCD adder using IC 7483 (10)
- Q3.** A) Design **MOD- 11** ripple counter using suitable flip-flop. (7)  
 B) Convert the following decimal number into binary, octal & hexadecimal
- $(555)_{10}$
  - $(138)_{10}$
  - $(79)_{10}$
- C) Why transistor biasing is required, state factors required for it (4)
- Q4** A) Draw truth table of full subtractor & realize using 3-8 decoder (10)  
 B) Draw the circuit diagram of voltage divider bias circuit using CE configuration  
 And explain how it stabilizes the operating point (10)
- Q5.** a)  $Y=ABC+BC'D+A'BC$  & realize using gates (6)  
 a) Explain parallel I/P serial output shift register (6)  
 b) Minimize the following expression using **only one** 8:1 MUX.  

$$F(A,B,C,D)=\sum m(1,2,9,10,11,14,15)$$
 (8)
- Q6.** Write short notes on **any four** (20)
- BCD & excess-3 codes
  - Current mirror circuit
  - Ring counter
  - ALU
  - Modelling styles in VHDL