

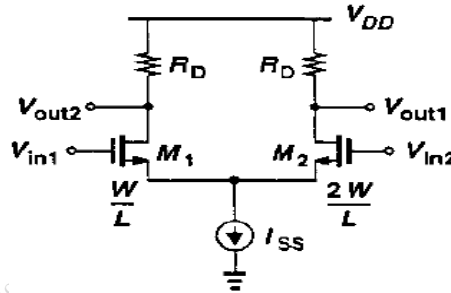
Time: 3 Hours

Max Marks: 80

- N.B. 1) Question No.1 is compulsory  
 2) Solve any three questions from the remaining questions.  
 3) Assume suitable data if necessary.

1 Solve the following.

- (a) Analyze following circuit to get voltage gain equation if M2 is twice wide as that of M1 and  $V_{in1}=V_{in2}$  5



- (b) Explain the concept of switched capacitor circuit 5  
 (c) Compare performance of various op-amp topologies 5  
 (d) Explain System on Chip and System in Package. 5
- 2 (a) Design two stage operational amplifiers that meet the following specifications 20  
 with a phase margin of 60. Assume the channel length is to be  $1\mu\text{m}$ ,  $K_N' = 100\mu\text{A}/\text{V}^2$ ,  $K_P' = 20\mu\text{A}/\text{V}^2$ ,  $V_{TN} = |V_{TP}| = 0.5\text{V}$ ,  $\lambda_N = 0.06\text{V}^{-1}$ , and  $\lambda_P = 0.08\text{V}^{-1}$   $A_v > 5000\text{v/v}$ ,  $V_{DD} = 2.5\text{V}$ ,  $V_{SS} = -2.5\text{V}$ ,  $\text{GBW} = 5\text{MHz}$ ,  $C_L = 10\text{pf}$ ,  $\text{SR} > 10\text{v}/\mu\text{sec}$ ,  $V_{out\text{ range}} = \pm 2\text{V}$ ,  $\text{ICMR} = -1\text{ to }2\text{V}$ ,  $P_{\text{diss}} \leq 2\text{mw}$ .
- 3 (a) Derive expression for voltage gain  $A_V$  and output resistance  $R_o$  of source 10  
 follower stage.  
 (b) Compare full custom and semi-custom design in terms of its trade-off and 5  
 applications.  
 (c) Explain Non-ideal effects in PLL. 5
- 4 (a) Derive equation of differential gain, common mode gain and CMRR of 10  
 differential amplifier.  
 (b) Explain White & Flicker noise in MOSFET. Derive equation for output and 10  
 input referred noise voltage of CS stage
- 5 (a) Draw and explain AMS design flow. 10  
 (b) Draw and explain discrete time integrator along with the output waveform. 10

6 Write short note on **any four**

- (a) Band Gap references
- (b) Cascode current mirror circuit.
- (c) Advantage and disadvantages of DLL
- (d) Stability and frequency compensation of two stage Opamp
- (e) Performance parameters of VCO

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