

(Time: 3 Hours)

Max Mrks:80

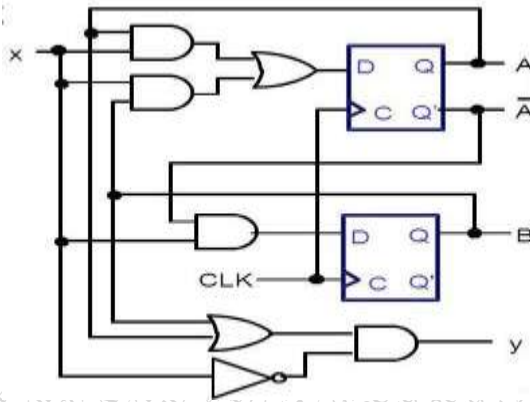
N.B:1) Question no. 1 is compulsory.

- 2) Attempt any three out of the remaining five questions.
- 3) Use suitable data, wherever necessary.

Q1. Attempt the following questions.

- (A) Differentiate between Mealy and Moore machine. (5)
- (B) Draw the Standard symbols for ASM Charts. (5)
- (C) Differentiate between signal and Variable. (5)
- (D) Explain what Entity in VHDL is. (5)

Q2. (A) Analyze the clocked synchronous machine given below. Write excitation equations, transition table and state/output table. Also draw the state diagram. (10)



(B) Design a mealy detector to detect a sequence 1101 using D flip-flops and logic gates. (10)

Q3. (A) Design a counter which counts the count from 3 to 12 using IC 74163. (10)

(B) Design MOD-12 Counter using IC 7493 and logic gates. (10)

Q4. (A) Design a circuit with optimum utilization of PLA to implement the following functions. (10)

$$F1 = \sum m(0,2,5,8,9,11)$$

$$F2 = \sum m(1,3,8,10,13,15)$$

$$F3 = \sum m(0,1,5,7,9,12,14)$$

B) Eliminate redundant states and draw reduced state diagram. (10)

PS	NS		Out Put Y
	X=0	X=1	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	G	0
F	E	D	0
G	F	G	0

Q5. (A) Write a VHDL code for JK flip-flop. (10)

(B) Write a VHDL code for 3:8 decoder with active low output. (10)

Q6. (A) Write a note on CPLD. (10)

(B) Draw the data unit for the following RTL description (10)

Module; Data Mover

Memory: A[2]; B[2]; C[2].

Inputs : X[2].

Outputs : Z[2].

1.  $A \leftarrow X$ .
2.  $C \leftarrow \bar{A}$ .
3.  $B \leftarrow C[0], C[1]$ .
4.  $C \leftarrow A \vee B$ .
5.  $Z = C$ .