Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5152]-577

S.E. (Information Technology) (Second Semester)

EXAMINATION, 2017

PROCESSOR ARCHITECTURE AND INTERFACING

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :— (*i*) Neat diagrams must be drawn wherever necessary.

(*ii*) Figures to the right indicate full marks.

(*iii*) Assume suitable data, if necessary

1. (*a*) Explain significance of Assembler, Linker, Debugger and Emulator. [7]

(*b*) Explain significance of call gates with its format. [5]

Or

2. (*a*) Explain significance of GDT, LDT and IDT. in 80386 with diagram. [7]

(*b*) Explain difference between Macro and Procedure. [5]

3. (*a*) Explain internal memory structure of 8051. [5]

(*b*) Draw diagram of Non-pipelined read cycle of 80586 and explain. [7]

P.T.O.

Or

4. (*a*) List features of 8051 Microcontroller. Compare Microcontroller with Microprocessor. [5]

(*b*) What is Multitasking ? Explain with diagram. [7]

5. (*a*) Explain significance of various ports [P_0 to P_3] in 8051. [7]

(*b*) Explain significance to TCON and TMOD with format. [6]

Or

6. (*a*) Explain interrupt structure of 8051 with diagram. [7]

(*b*) Explain Mode 0 and Mode 1 of timer in 8051. [6]

7. (*a*) How to configure port 1 and port 2 for 2-digit seven segment display ? Explain with diagram and instruction. [7]

(*b*) Draw interfacing diagram of DAC with 8051. Explain. [6]

Or

8. (*a*) Draw interfacing diagram of 8051 with external program memory as 4k × 8 and external data memory as 2k × 8. [7]

(*b*) Draw and explain functional block diagram of 8255. [6]