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[4857]-1087

S.E. (Information Technology) (Second Semester)

EXAMINATION, 2015

PROCESSOR ARCHITECTURE AND INTERFACING

(2012 PATTERN)

Time : Two Hours

Maximum Marks : 50

N.B. :- (i) Answer Q. 1 or Q. 2, Q. 3 or Q. 4, Q. 5 or Q. 6,
and Q. 7 or Q. 8.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) Draw programmer's model of 80386 processor and state the use of all registers. [6]

(b) Explain various signals associated with coprocessor interface of 80386. [6]

Or

2. (a) State the use of Assembler, Linker, Debugger, Loader, Emulator and state how the assembly program is assembled using MASM with example. [6]

(b) Explain pipelined read bus cycle with neat diagram. [6]

P.T.O.

3. (a) Draw the flow-charts : [6]
(i) Switching from real to protected mode
(ii) Switching from protected to real mode.
(b) Explain the difference among three operating modes of 80386. [6]

Or

4. (a) Draw and explain formats of page directory entry and page table entry. [6]
(b) What is dual core processor ? Explain features of dual core processor. [6]

5. (a) List any *six* features of 8051 microcontroller and compare microcontroller with microprocessor. [7]
(b) Explain any *three* different addressing modes of 8051 with suitable examples. [6]

Or

6. (a) State the use of SCON and TCON registers. Draw and explain their structures. [7]
(b) Explain the use of the following pins of 8051 : [6]
(i) $\overline{\text{PSEN}}$
(ii) $\overline{\text{EA}}$
(iii) TXD.

7. (a) Explain different sources of interrupts in 8051. Draw interrupt structure of 8051. [7]
- (b) List all SFRs of timer programming and draw and explain PCON register. [6]

Or

8. (a) List timer/counter modes of 8051 and draw and explain mode 0 and mode 2. [7]
- (b) Draw and explain a minimal 8051 based system that interfaces a 4×4 matrix keyboard to port 1 and port 2. [6]

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