

Total No. of Questions : 12]

SEAT No. :

P1393

[4759] - 95

[Total No. of Pages : 3

**B.E. (Electronics & Telecommunication)**

**MICROELECTROMECHANICALSYSTEMANDSYSTEMSONCHIP  
(2008 Course) (Semester - I) (Elective - II) (404185)**

*Time : 3 Hours]*

*[Max. Marks : 100*

*Instructions to the candidates:*

- 1) *Attempt 3 questions from each section.*
- 2) *Attempt from section - I: Q1 or Q2, Q.3 or Q.4, Q.5 or Q.6, and from section - II: Q.7 or Q.8, Q.9 or Q.10, Q.11 or Q.12.*
- 3) *Neat diagrams must be drawn wherever necessary.*
- 4) *Assume suitable data if necessary.*
- 5) *Figures to the right indicates marks.*

**SECTION - I**

- Q1)** a) Point out the difference between MEMS and Microsystems. [8]  
b) What are the general desirable characteristics of MEMS? [8]

OR

- Q2)** a) Draw and explain functional block diagram of MEMS. [8]  
b) Explain photolithography process in detail. [8]
- Q3)** a) Justify "Silicon- an ideal substrate material for MEMS". [8]  
b) What is SU-8 photoresists? Write brief about it. [8]

OR

- Q4)** a) What are the silicon compound which are used in MEMS fabrication? Describe any one of them. [8]  
b) What do you mean by piezoresistance? Can we use silicon for the same? Write down mathematical expression for it. [8]

*P.T.O.*

- Q5) a)** Point out major technical issues in BioMEMS products. [9]
- b) Explain glucose monitoring and drug delivery system. [9]

OR

**Q6)** Write short note on: [18]

- a) Chemical sensors
- b) Micro accelerometers
- c) Magnetic Actuators

**SECTION - II**

- Q7) a)** What is SOC? Write various components of SOC. [8]
- b) Draw typical architecture of SOC. [8]

OR

- Q8) a)** Point out difference between SOC and processors on chip. [8]
- b) Justify “SOC increases chip complexity”. [8]

- Q9) a)** What is the difference between wet & dry etching? [8]
- b) What are the merits and demerits of behavioural synthesis? [8]

OR

- Q10) a)** Write various layout strategies for IC design. [8]
- b) What is LEGAL? Explain LEGAL algorithm steps. [8]

- Q11)a)** Explain various packaging technologies and explain each in detail. [9]
- b) What are the issues in testing of core based systems on chip? Explain features of co-design tool. [9]

OR

- Q12)a)** Explain generic test generation procedure with flow chart. Explain embedded core based system on chip test strategies. [9]
- b) Explain the terms: [9]
- i) Defects and fault method
  - ii) Fault simulation



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