Total No. of Questions : 12]

SEAT No. :

[Total No. of Pages : 3

P3011

B.E. (Semester - II)

ELECTRONICS AND TELECOMMUNICATION

Microelectromechanical System and Systems on Chip

(2008 Pattern) (Elective - II)

Time : 3 Hours] *[Max. Marks : 100*

Instructions to the candidates:

1) ***Answers to the two sections should be written in separate answer books.***
2) ***Answer from Section - I : Q1 or Q2, Q3 or Q4, Q5 or Q6 and from section -II : Q7 or Q8, Q9 or Q10, Q11 or Q12.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right side indicate full marks.***
5) ***Use of calculator is allowed.***
6) ***Assume suitable data, if necessary.***

SECTION - I

Q1) a) Explain basic working principal of micro pressure sensor. What are major problems in these sensors? **[8]**

b) What are scaling laws of miniaturization? Explain with example scaling law in geometry of a MEMS device. **[8]**

Q2) a) Explain mechanical properties of materials. **[8]**

b) What is LEGAL? Explain LEGAL algorithm steps. What kind of improvement inculcated in LEGAL in context to earlier routing algorithms? **[8]**

Q3) a) Compare GaAs Vs Silicon. **[8]**

b) What is polymer? Explain their characteristics and give principal applications of polymers. **[8]**

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Q4) a) Explain working principal of silicon piezoresistors? **[8]**

b) Explain the concept of : **[8]**

i) Mobility

ii) Resistivity in context to Piezo crystal

Q5) a) Explain how biosensor is used for glucose concentration? **[9]**

b) Explain in general optical and optical silicon properties. **[9]**

Q6) a) Explain working principal of chemical sensors. **[9]**

b) Explain various technological aspects of sensors. **[9]**

SECTION - II

Q7) a) Explain in detail schematic of an MPEG2 encoder for terrestrial transmission. **[8]**

b) Explain main characteristics of VLSI technology that are leading to overall organization of microprocessors. **[8]**

Q8) a) What are the important parameters which define wafer level bonding? Also give its significance. **[8]**

b) Explain in detail new ways for speeding up execution of instructions. **[8]**

Q9) a) Which features of designer should look in layout synthesis tool? **[8]**

b) Explain working of CVD? Which new CVD process is used to overcome drawbacks of CVD process? **[8]**

Q10) a) What are the goals of layout synthesis tool? Which technical issues CMOS layout tool handles? Differentiate horizontal versus vertical routing. **[8]**

b) Explain cycle dependency and generation of problem with suitable example in context to cell placement. **[8]**

Q11) a) Which features are inculcated in co-design tool? Explain design steps for co-design. **[9]**

b) What are the issues in testing of core based systems on chip? **[9]**

Q12) a) Explain generic test generation procedure using flowchart. **[9]**

b) What reliability issues are crop up in packaging? Which factors leads failures in packaging? **[9]**

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