Total No. of Questions : 8]

SEAT No. :

P4832

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# [5152]-569
# S.E. (Computer) (Semester - IV)
# MICROPROCESSOR
# (2015 Pattern)

*Time : 2 Hours]* *[Maximum Marks : 50*

***Instructions to the candidates:***

1) ***Answer Question No.1 or 2, 3 or 4, 5 or 6 and 7or 8.***
2) ***Neat diagram must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

***Q1)*** a) What is the use of following instructions? **[2]**

i) Wait

ii) Lock

b) Explain segment address translation in detail. **[4]**

c) Draw and explain segment descriptor. **[6]**

OR

***Q2)*** a) What is the use of Direction Flag? **[2]**

b) Draw and explain the system address and system segment registers. **[4]**

c) Explain the following instructions, mention flags affected: **[6]**

i) CWD

ii) BT

iii) LAHF

***Q3)*** a) List the registers and data structures that are used in multitasking. **[2]**

b) Differentiate between memory mapped I/O and I/O mapped I/O. **[4]**

c) Explain what happens when an interrupt calls a procedure as an interrupt handler. **[6]**

OR

***Q4)*** a) Write the two mechanisms that provide protection for I/O functions. **[2]**

***P.T.O***

b) What is IDT and how to locate IDT? **[4]**

c) Explain the different exception conditions-Faults, Traps and Aborts. **[6]**

***Q5)*** a) Write short note on "Task Switch Breakpoint". **[3]**

b) Write short note on "Protection within a V86 task". **[4]**

c) Explain various debugging features of 80386. **[6]**

OR

***Q6)*** a) Write short note on "General Detect Fault". **[3]**

b) Which bit of EFLAGs indicates V86 mode? Explain, how hardware and software cooperate with each other to emulate V86 mode? **[4]**

c) Explain, how test registers are used in testing TLB? **[6]**

***Q7)*** a) Explain following signals **[3]**

i) ADS#

ii) READY#

iii) NA#

b) Write note on CLK2 and internal processor clock. **[4]**

c) Which data types are supported by 80387? **[6]**

OR

***Q8)*** a) Explain following signals **[3]**

BE0# through BE3#.

b) Explain following signals **[4]**

i) PEREQ

ii) BUSY#

iii) ERROR#

c) Draw read cycle with pipelined address timing. **[6]**

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