University of Mumbai

T.E Third Year 2013 - 2014 May

Semester 6 (TE Third Year)

Advanced Microprocessor

www.shaalaa.com

T.E. Comp Sem VI (Rev) M-2014 20/5/14

Sub - Adv. Microprocessor

QP Code : MV-18124

(3 Hours) **[Total Marks : 100**

N.B.:

1. Q. 1 is compulsory.
2. Answer any four questions from remaining questions.
3. Assume suitable data if necessary.
4. Figures to the right indicate full marks.

Q.1.	a)	Explain instruction pairing on Pentium processor.	05
	b)	Explain control and structural hazards with respect to superscalar processor architecture.	05
	c)	Write short note on RISC evaluation.	05
	d)	Explain IA 64 Itanium processor architecture in brief.	05
Q.2.	a)	What is descriptor? Explain Code and Data segment descriptor with neat diagram.	10
	b)	Explain protection mechanism implemented on 80386DX..	10
Q.3.	a)	Explain Integer pipeline of Pentium processor.	10
	b)	Explain Pentium processor architecture with block diagram.	10
Q.4.	a)	Explain Pentium II software changes in detail.	10
	b)	Explain branch prediction logic implemented on Pentium processor.	10
Q.5.	a)	Explain cache/MMU organization of SuperSPARC processor.	10
	b)	Explain, in detail, register file of SPARC processor.	10
Q.6.	a)	Explain the features of USB bus. Also, explain features of ISA bus.	10
	b)	Write short note on I. ATA II. SCSI	10
Q.7.	Write short note on		
	a)	Cache memory organization	05
	b)	Pentium IV processor	05
	c)	Systolic architecture	05
	d)	Operating modes of 80386	05
