B. E. Sem VIII (old) (ETRX). 17/12/15

A VLSI

QP Code : 2613

(Revised Course)

Duration: 3hrs. Total marks: 100

NB:
Question No. 1 is compulsory,
Attempt any four out of remaining six questions,
Assume any suitable data whenever required and justify the same.

1. a) Explain Manchaster carry circuits (5)
   b) Explain how ESD (electro-static discharge) affect the MOSFET (5)
   c) Write Verilog code for 8 bit counter. (5)
   d) Draw and explain Carry save adder (5)

2. a) Determine intrinsic gate capacitance with t_{ox}=150Å, V_G=3.3V. ε=3.9X8.854x10^{-14}F/cm,.if W=4μm,L=2μm. (10)
   b) Implement following function using PLA (10)

$$X = ac + b\bar{c}$$
$$Y = a\bar{b}c + \bar{a}b\bar{c}$$
$$Z = ab + \bar{a}\bar{b}$$

3. a) Explain various technique of clock generation and clock stabilization. (10)
   b) Draw 4 X 4 pseudo-nMOS ROM array circuitry having stored following data 0011, 1010, 1100, 0101. Also list the no. of address pins, data pins and word lines (10)

4. a) What is the need of sizing routing conductors, how does it affects RC delay explain ? (10)
   b) Explain EEPROM using floating gate NMOSFET. (10)

5. a) Give and explain CLA Adder with generate and propagate term with their Verilog code. (10)
   b) Explain in detail the input protection circuit for CMOS, also explain output circuit with I/O circuit. (10)

6. a) Give and explain single phase clock system and explain its drawback. (10)
   b) Give various important parameters affecting switching performance of CMOS circuit. Suggest method to improve it. (10)

7. Write short note (any 3) (20)
   a) Reliability issues in CMOS circuits.
   b) Low power design consideration
   c) Switch capacitor amplifier.
   d) H tree clock distribution.

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