B.E (ETRx) VIII for 14/5/2015 1/2

Advance VLSI Design

Q.P. Code : 8014

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. 1 is compulsory.
(2) Answer **Any Four** questions out of remaining questions.
(3) Assume any suitable data wherever required.

1. a) Explain Charge sharing and charge leakage problem of dynamic Logic circuit. 5

   b) Explain cross talk in integrated circuits. 5

   c) Explain EEPROM using floating gate NMOSFETS. 5

   d) Compare clock skew and jitter. 5

2. a) What is effect of interconnect parasitic on delay? How delay can be reduced ? What is Elmore delay model? 10

   b) Give and explain single phase clock system and explain its drawback. 10

3. a) Implement 4 bit adder using Carry Look Ahead (CLA) principle. 10

   b) State the need of input and output circuit. Explain with neat diagram the schematic and design considerations for the same. 10

4. a) Explain frequency compensation in operational amplifier. 10

   b) Implement the following function using NOR-NOR implementation for a PLA. 10
   F1= abc+ a'b'c'
   F2= a'c' + a'b
   F3= ab' +ac

5. a) What are the different clock generation schemes employed in VLSI systems. Discuss 'H' tree clock distribution in high density CMOS circuits. 10

   b) Draw schematic for 6T SRAM cell and explain its stability criteria. Also draw and discuss its butterfly curve. 10

Q.P. Code : 8014

6. a) Draw 4x4 NOR based ROM array circuitry stored following data 1011,1001,0101,0011. **10**

b) Give and explain the maximum and minimum frequency calculation of clock signal which determine the data transfer rate through cascade system. **10**

20

Q7. Write short notes on (any three)

a) Low power design consideration.
b) Carry skip adder.
c) Interconnect scaling.
d) Switched capacitor circuit.
