Advanced VLSI Design (Rev)
BE ETRX Sem-VIII
31/5/14 11.00 to 2.00

QP Code : MV-19048

(3 Hours) **[Total Marks : 100**

N.B. : (1) Questions **No. 1** is **compulsory.**
(2) **Attempt** any **four** out of remaining **six** questions
(3) Assume any suitable data whenever required and justify the same.

1. (a) Give and explain the routing capacitance with fringing field effect. **5**
   (b) Give and explain carry save adder. **5**
   (c) Write specification of Row Decoder, Column Decoder and MUX/DMUX used in 64K X 8 SRAM. **5**
   (d) Give and explain two techniques to improve the minimum frequency requirement of clock signal. **5**

2. (a) Draw and explain full adder using dual rail complementary pass transistor logic. **10**
   (b) Give various important parameters affecting switching performance of CMOS inverter. Suggest methods to improve it. **10**

3. (a) Explain in detail sizing of routing conductor with respect to metal migration and ground bounce /power supply drop. **10**
   (b) Draw 1T DRAM cell and explain its write, read, hold and refresh operation. **10**

4. (a) Draw and explain CMOS two-stage OP-AMP. **10**
   (b) Explain various technique of clock generation. Discuss "H" tree clock distribution. **10**

5. (a) Draw three variable-three output PLA and programme it with following functions: **10**

   $fx = ac + be$
   $Fy = abc + abc$
   $Fz = ab + ab$

   (b) Give and explain interconnect scaling. **10**

6. (a) Give and explain single phase clock system and explain its drawback. **10**
   (b) Explain need of input protection and give the input protection circuits. **10**

7. Write short note on (any three) **20**
   (a) Switch Capacitor amplifier
   (b) Sense amplifier
   (c) Low power design consideration
   (d) Floating gate MOSFET.
