B.E. Sem VII (R) (O) ETRX. 02/6/2015

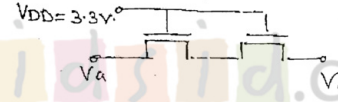
VLSI Design

QP Code : 8599

(3 Hours) **[Total Marks : 100**

N.B: (1) Question No.**1** is **Compulsory**.
(2) Attempt any **Four** out of remaining **six** questions.
(3) Assume suitable **data** wherever **necessary**

1. Attempt any **four** : **20**
   (a) Compare ion implantation and diffusion.
   (b) Draw VTC of three CMOS inverter with $K_R = 1$, $K_R < 1$ & $K_R > 1$.
   (c) Two n-MOS transistors (M1 & M2) connected in series shown in fig find output voltage for
      i) Va = 2.7 V, ii) Va = 3V.
      $V_{TH} = 0.7V$



   (d) Explain MOSFET works as a capacitor. **10**

2. (a) Explain operation of CMOS inverter with clearly mentioning the five cases given below. **10**
      (i) $V_{in} < V_{TO,n}$
      (ii) $V_{in} = V_{IL}$
      (iii) $V_{in} = V_{IH}$
      (iv) $V_{in} > V_{DD} + V_{TO,P}$
      (v) $V_{in} = V_{TH}$

   (b) Draw the p-well CMOS inverter and explain the latch up effect in it. What are remedies to avoid latch up problem. **10**

3. (a) Calculate threshold voltage V_{TO} at $V_{SB} = 0$ for a polysilicon gate n-channel MOS transistor with following parameters. **10**
      $N_A = 10^{16} cm^{-3}$, $N_D = 2 \times 20^{20} cm^{-3}$
      $t_{ox} = 200$ °A $N_{SS} = 5 \times 10^{11} cm^{-2}$
   (b) Write a verilog code for 4 × 4 barrel shifter. **10**

4. (a) Draw a circuit diagram, stick diagram and layout for following equation 10
$Y = \overline{A \cdot B \cdot C}$
Use CMOS technology.

(b) Consider a CMOS inverter circuit with the following parameters 10
$V_{DD} = 3.3V$ $V_{TO,n} = 0.6V$ $V_{TO,p} = -0.7V$
$\mu_n C_{ox} = 60\mu A/V^2, (W/L)_n = 8$
$\mu_p C_{ox} = 20\ \mu A/V^2, (W/L)_p = 12$
Calculate the noise margin.

5. (a) Describe the hot electron and short channel effect in MOS device. Also explain their effect on MOS characteristic. 10

(b) Explain necessity of design rules ? Explain λ based design rules in detail. 10

6. (a) Define scaling. Explain constant voltage and constant field scaling in detail. 10

(b) Explain the method to design 4:1 MUX using NMOS pass transistor logic. Draw complete stick diagram. 10

7. Write a short notes on (any **three**) : 20
(i) MOS CV characteristics
(ii) VLSI design flow
(iii) Semicustom and full custom design
(iv) Transistor sizing.