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10CS33

Third Semester B.E. Degree Examination, Dec.2015/Jan.2016
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. What is Logic gate? State and prove De Morgan's theorems. **(07 Marks)**

b. Describe positive and negative logic. Prove "positive OR" logic equal to "Negative AND" logic. **(05 Marks)**

c. Implement the following function by using : i) Nand gates only ii) NOR gates only.
$Y = \overline{((A + B).C)}.D$ **(08 Marks)**

2 a. Find the minimal SOP and minimal POS of the following Boolean function using K - Map.
$f(a, b, c, d) = \Sigma_m (6, 7, 9, 10, 13) + d(1, 4, 5, 11)$. **(08 Marks)**

b. Using Q.M method simplify the following expression and realize it by using Nand logic only. $f(a, b, c, d) = \Sigma(0, 3, 5, 6, 7, 11, 14)$. **(10 Marks)**

c. Write a note on Static Hazard. **(02 Marks)**

3 a. Construct 8:1 multiplexer using only 2:1 multiplexer. **(06 Marks)**

b. Mention the three differences between decoder and demultiplexer. **(03 Marks)**

c. Write the four comparisons between PLA and PAL. **(04 Marks)**

d. Implement the following function using PLA : **(07 Marks)**
$A(x, y, z) = \Sigma m (1, 2, 4, 6)$; $B(x, y, z) = \Sigma m (0, 1, 6, 7)$; $C(x, y, z) = \Sigma m (2, 6)$.

4 a. With logic diagram and truth table, explain the working of master slave (J, K) flip flop. **(06 Marks)**

b. Draw the logic truth table and timing diagram of positive edge triggered D – flip flop. **(06 Marks)**

c. Write the verilog code for positive edge triggered J.K flip flop. **(03 Marks)**

d. With neat diagram, explain the working principles of Switch De bouncer circuit. **(05 Marks)**

PART - B

5 a. Write a note on classifications of Registers. **(04 Marks)**

b. With neat diagram and timing diagram, explain the working of Serial in – Serial out register. For explanation construct 4 bit register using J.K flip flops. **(10 Marks)**

c. Write a Verilog code for : i) Switched tail counter ii) Shift registers of 5 bits constructed using D-flip flops. **(06 Marks)**

6 a. Write the comparison between Synchronous and Asynchronous counter. **(04 Marks)**

b. Design : i) a divide by 78 counter using 7493 and 7492 IC ii) modulo 120 counter using 7490 and 7492 IC. **(08 Marks)**

c. Design a mod 6 counter using J.K flip flops and K – map simplification method. **(08 Marks)**

7 a. Explain the difference between Mealy model and Moore model. **(05 Marks)**

b. Design a Mealy type sequence detector to detect a serial i/p sequence of 101. **(10 Marks)**

c. How does state transition diagram of a Moore machine differ from Melay machine? **(05 Marks)**

8 a. Explain with neat diagram, successive approximation A/D converter. **(06 Marks)**

b. Explain with neat diagram, counter method of A/D conversion. **(06 Marks)**

c. Write short notes on :
i) Binary loader ii) Differences between D/A and A/D converters. **(08 Marks)**

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